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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,481	GODA ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/145,122.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: element 39 (see, for example, FIG. 3B). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second post-oxidation film and third post-oxidation film must be shown or the feature(s) canceled from the claim(s). In FIG. 13 (the only figure which shows the oxidized region 37' being provided in a surface of the silicon nitride film, see last two lines of claim 19), it shows first post-oxidation films 36 and insulating film 37, but no second post-oxidation film and third post-oxidation film. It is also unclear

whether the first post-oxidation films 36 are one film or a plurality of films since the figures only show one first post-oxidation film 36. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 21 is objected to because of the following informalities: the limitation "atom" should be plural. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 19 thru 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what the second post-oxidation film and third post-oxidation film is referring to in claims 19 and 32 since there are only post oxidation film (first post-oxidation films) 36, silicon nitride film (insulating film) 37, and oxidized region 37' on the gate electrodes 35, 41. There does not appear to be any second post-oxidation film provided on the gate electrode 35 of the selection transistor ST or a third post-oxidation film provided on the gate electrode 41 of the peripheral transistor CT. See, for example, FIG. 13.

In claim 22, and 32, it not clear how the concentration of the hydrogen gradually "becomes higher" from the surface of the silicon nitride film since the surface of the silicon nitride is directly oxidized and therefore would have "more" reduced hydrogen than regions underneath the surface (in the silicon nitride film).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Insofar as definite, claims 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue 5,449,634 in view of Koyama 5,348,904 in view of Yamaha 5,786,638.

Inoue discloses (see, for example, FIG. 2n) a non-volatile semiconductor memory device comprising a semiconductor substrate 1, peripheral circuit active region (peripheral circuit region) 21, memory cell active region (memory cell region) 22, plurality of memory cell transistors (plurality of erasable and programmable memory cell transistors), third electrode layer (gate electrode) 12, a memory cell transistor (selection transistor), peripheral transistor, third insulating layer (second post-oxidation film) 15, first interlayer insulating film (third post-oxidation film) 8. Inoue does not disclose first post-oxidation films each provided on the gate electrode of all of the plurality of erasable and programmable memory cell transistors. However, Koyama discloses (see, for example, FIG. 14) a semiconductor memory device comprising peripheral circuit area 801, memory cell array area 800, and silicon oxide film (first post-oxidation films) 14. The silicon oxide film covers the gate electrodes 12, and serves as an interlayer insulator. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have first post-oxidation films each provided on the gate electrode of all of the plurality of erasable and programmable memory cell transistors in order to cover the gate electrodes, and have an interlayer insulator.

Inoue in view of Koyama does not disclose an insulating film covering the plurality of erasable and programmable memory cell transistors, wherein the insulating film comprises a silicon nitride film, and the oxidized region is provided in a surface of the silicon nitride film. However, Yamaha discloses (see, for example, FIG. 1) a semiconductor device comprising a silicon nitride film (insulating film) 24, and a silicon oxide film (oxidized region) 18a. Yamaha discloses (see, for example, column 2, lines 20-24) the silicon nitride and silicon oxide film prevent moisture from permeating into the active region. Therefore, it would have been obvious

to one of ordinary skill in the art at the time of invention to have an insulating film covering the plurality of erasable and programmable memory cell transistors, wherein the insulating film comprises a silicon nitride film, and the oxidized region is provided in a surface of the silicon nitride film in order to prevent moisture from permeating into the active region.

Regarding claim 20, Inoue in view of Koyama in view of Yamaha does not disclose a thickness of the oxidized region of the silicon nitride film being not smaller than 1 nm and not larger than 10 nm. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the thickness of an oxidized region of the silicon nitride film in order to prevent moisture from permeating into an active region and having proper insulation. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have a thickness of the oxidized region of the silicon nitride film being not smaller than 1 nm and not larger than 10 nm because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the thickness of the oxidized region of the silicon nitride film in order to prevent moisture from permeating into an active region and to have proper insulation. See In re Aller, 105 USPQ 233.

8. Claims 21, 22, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue '634 in view of Koyama '904 in view of Yamaha '638 as applied to claims 19, and 20 above, and further in view of Huanga et al. 5,670,431. Inoue in view of Koyama in view of Yamaha does not disclose the silicon nitride film containing hydrogen with a concentration not larger than 3×10^{21} atom/cm^3. However, Huanga discloses (see, for example, column 6, lines 10-15) a silicon nitride layer formed using hydrogen reactants. It would have been obvious to

one of ordinary skill in the art at the time of invention to have the silicon nitride film containing hydrogen in order to have a method that adequately forms a silicon nitride film. Inoue in view of Koyama in view of Yamaha in view of Huanga does not disclose hydrogen with a concentration not larger than 3×10^{21} atom/cm^3. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the concentration of hydrogen in order to consequently form a silicon nitride film. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have hydrogen with a concentration not larger than 3×10^{21} atom/cm^3 because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the concentration of hydrogen in order to form a silicon nitride film. See In re Aller, 105 USPQ 233.

9. Claims 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue '634 in view of Koyama '904 in view of Yamaha '638 as applied to claims 19, and 20 above, and further in view of Yamazaki et al. 6,472,684. Inoue in view of Koyama in view of Yamaha does not disclose the gate electrode of each of the plurality of erasable and programmable memory cell transistors, the selection transistor, and the peripheral transistor containing a metal or a metal silicide. However, Yamazaki discloses (see, for example, column 13, lines 9-13) gate electrodes made of various materials such as tungsten (metal). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate electrode of each of the plurality of erasable and programmable memory cell transistors, the selection transistor, and the peripheral transistor containing a metal or a metal silicide in order to have a gate electrode of adequate conductivity.

10. Claims 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue '634 in view of Koyama '904 in view of Yamaha '638 as applied to claims 19, and 20 above, and further in view of Kleine 6,162,682, and further in view of Yamazaki et al. 6,472,684. Inoue in view of Koyama in view of Yamaha does not disclose the peripheral transistor being a stacked gate structure including a floating gate and a control gate. However, Kleine discloses (see, for example, Fig. 8 (e)) a periphery circuit transistor 860 comprising a stacked gate structure wherein the stacked gate structure comprises a first conducting layer (floating gate) 820, and second conducting layer (control gate) 850. It would have been obvious to one of ordinary skill in the art at the time of invention to have the peripheral transistor being a stacked gate structure including a floating gate and a control gate in order to form the peripheral transistor in another way that is similar to the process steps of the other transistors formed, thereby saving manufacturing time.

Inoue in view of Koyama in view of Yamaha in view of Kleine does not disclose the control gate comprising a metal or a metal silicide. However, Yamazaki discloses (see, for example, column 13, lines 9-13) gate electrodes made of various materials such as tungsten (metal). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate electrode of each of the plurality of erasable and programmable memory cell transistors, the selection transistor, and the peripheral transistor containing a metal or a metal silicide in order to have a gate electrode of adequate conductivity.

11. Claims 27 thru 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue '634 in view of Koyama '904 in view of Yamaha '638 as applied to claims 19, and 20 above,

and further in view of Endoh 5,677,556. Inoue in view of Koyama in view of Yamaha does not disclose the memory cell transistor being series-connected to each other. However, Endoh discloses (see, for example, column 1, lines 19-24) a plurality of memory cells connected in series with each other to form an NAND cell type. It would have been obvious to one of ordinary skill in the art at the time of invention to have the memory cell transistor being series-connected to each other in order to form a more intricate memory structure such as an NAND cell type.

Regarding the limitation "contact plug", see, for example, FIG. 2n, wherein Inoue discloses a metal electrode (contact plug) 20.

Regarding claim 31, Inoue in view of Koyama in view of Yamaha does not disclose an AND EEPROM. However, Endoh discloses (see, for example, column 9, lines 33-35) an AND-type EEPROM memory cell in addition to the NAND-type memory cell. It would have been obvious to one of ordinary skill in the art at the time of invention to have an AND EEPROM (or NAND EEPROM) in order to form an intricate memory cell structure for storage.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
March 21, 2005